IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellant:	Snyder	Patent Application
Serial:	10/033,027	Group Art Unit: 2183
Filed:	10/22/2001	Examiner: Daniel H. Pan

For: PROGRAMMABLE MICROCONTROLLER ARCHITECTURE

Appeal Brief

CYPR-CD00232/ACM/NAO

Table of Contents

Real Party in Interest

The assignee of the present invention is Cypress Semiconductor Corporation.

Related Appeals and Interferences

There are no related appeals or interferences known to the Appellant.

Status of Claims

Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57-59 are pending.

Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57-59 are rejected under 35 USC § 112, second paragraph. Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57-59 are rejected under 35 USC § 103(a).

Status of Amendments

All proposed amendments have been entered. An amendment subsequent to the final rejection has not been filed.

Summary of Claimed Subject Matter

One embodiment of the present claimed invention is directed to a programmable system on a chip comprising programmable analog and digital function blocks. Embodiments of the present invention provide an integrated system with a microcontroller and integrated circuits (IC), on a single chip to effectuate a system on a chip, including programmable analog and digital functionality and a microprocessor, and a method of configuring such an integrated system. Embodiments in accordance with the present invention also provides a system on a chip, which has sufficient flexibility to function in a very wide range of multiple applications, including applications wherein integrated analog functionalities are required. Further, embodiments in accordance with the present invention provides a method of programming and dynamically reconfiguring a system on a chip, and a system on a chip, which is so programmable and dynamically reconfigurable. Further still, embodiments in accordance with the present invention provides a system on a chip, which achieves the foregoing advantages and yet is relatively inexpensive and readily configurable, and easy to apply, use, and reconfigure.

Independent Claim 1 recites:

A microcontroller circuit comprising:

a bus;

a microprocessor coupled to said bus;

a memory coupled to said bus, wherein said memory comprises a non-volatile memory; and

a plurality of functional units coupled to said bus, wherein said non-volatile memory functions to program said functional units and wherein said plurality of functional units comprise:

an interconnect wherein said interconnect is dynamically configurable and programmable;

an analog functional block coupled to said interconnect wherein said analog function block is dynamically configurable and programmable to perform one or more of a plurality of various analog functions; and

a dynamically configurable and programmable digital functional block coupled to said interconnect, wherein said dynamically configurable and programmable digital functional block is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation.

Item 10 of Figures 1A and 1B of the instant specification illustrates embodiments of the present invention in accordance with this Claim. Explanation of these items is provided by the instant Specification at least at page 15, line 25, *et seq.*, *inter alia.*

Independent Claim 11 recites:

An integrated circuit comprising:

a bus;

a microprocessor coupled to said bus;

a memory coupled to said bus, wherein said memory comprises a non-volatile memory;

a plurality of functional units coupled to said bus, wherein said non-volatile memory stores code for programming said functional units and wherein said plurality of functional units comprise:

an interconnect wherein said interconnect is dynamically configurable and programmable;

an analog functional block coupled to said interconnect wherein said analog function block is dynamically configurable and programmable to perform one or more of a plurality of various analog functions; and

a dynamically configurable and programmable digital functional block coupled to said interconnect, wherein said dynamically configurable and programmable digital functional block is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation; and

an input/output coupling, wherein said integrated circuit comprises a microcontroller.

Item 10 of Figures 1A and 1B of the instant specification illustrates embodiments of the present invention in accordance with this Claim. Explanation of these items is provided by the instant Specification at least at page 15, line 25, *et seq.*, *inter alia.* In addition, Figure 3 shows the interconnects between analog blocks 20 in an array in accordance with one

embodiment of the present invention. Further, Figures 4A, 4B, 5, 6, 7, 8A and 8B, 9A, 9B, 10, 11, 12A, 12B, 13, 14A and 14B show a plurality of embodiments of an analog block. Still further, Figures 16, 18, 19, 20, 21, 22, 23, and 24 show a plurality of embodiments of a digital block.

Independent Claim 17 recites:

A microcontroller circuit, comprising:

a microprocessor;

a plurality of analog circuit blocks wherein said analog function block is dynamically configurable and programmable to perform one or more of a plurality of various analog functions;

a plurality of dynamically programmable digital circuit blocks wherein at least one of said dynamically programmable digital circuit blocks is coupled directly or indirectly to at least one of said dynamically programmable analog circuit blocks wherein at least a first one of said dynamically programmable digital circuit blocks is coupled directly or indirectly to at least a first one of said dynamically programmable analog circuit blocks, and at least a second one of said dynamically programmable digital circuit blocks and said dynamically programmable analog circuit blocks is coupled directly or indirectly to said microprocessor and wherein said coupling is achieved with an interconnect, wherein said interconnect is dynamically programmable and configurable, wherein each dynamically programmable digital circuit block is configurable to perform any one of a plurality of digital functions upon being configured with a single register write operation; and

a programmable non-volatile memory coupled directly or indirectly to said plurality of dynamically programmable digital circuit blocks and said plurality of dynamically programmable analog circuit blocks, said programmable non-volatile memory storing code for programming at least one of said programmable digital circuit blocks and at least one of said plurality of programmable analog circuit blocks.

Item 10 of Figures 1A and 1B of the instant specification illustrates embodiments of the present invention in accordance with this Claim. Explanation of these items is provided by the instant Specification at least at page 15, line 25, *et seq.*, *inter alia.* In addition, Figure 3 shows the interconnects between analog blocks 20 in an array in accordance with one embodiment of the present invention. Further, Figures 4A, 4B, 5, 6, 7, 8A and 8B, 9A, 9B, 10, 11, 12A, 12B, 13, 14A and 14B show a plurality of embodiments of an analog block. Still further, Figures 16, 18, 19, 20, 21, 22, 23, and 24 show a plurality of embodiments of a digital block.

Independent Claim 35 recites:

A microcontroller circuit, comprising:

a plurality of input and/or output blocks;

a plurality of programmable analog circuit blocks, wherein said analog circuit blocks are dynamically configurable and programmable to perform one or more of a plurality of various analog functions; and

a plurality of dynamically programmable digital circuit blocks, at least one of said programmable digital circuit blocks being coupled directly or indirectly to at least one of said programmable analog circuit blocks wherein at least one of said programmable digital circuit blocks and said programmable analog circuit blocks is coupled directly or indirectly to at least one of said input and/or output blocks, wherein each dynamically programmable digital circuit block is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation; and

a programmable non-volatile memory coupled to said plurality of programmable digital circuit blocks and said plurality of programmable analog circuit blocks, said programmable memory comprising data for programming at least one of said programmable digital circuit blocks and at least one of said plurality of programmable analog circuit blocks.

Item 10 of Figures 1A and 1B of the instant specification illustrates embodiments of the present invention in accordance with this Claim. Explanation of these items is provided by the instant Specification at least at page 15, line 25, *et seq.*, inter *alia*. In addition, Figure 3 shows the interconnects between analog blocks 20 in an array in accordance with one embodiment of the present invention. Further, Figures 4A, 4B, 5, 6, 7, 8A and 8B, 9A, 9B, 10, 11, 12A, 12B, 13, 14A and 14B show a plurality of embodiments of an analog block. Still further, Figures 16, 18, 19, 20, 21, 22, 23, and 24 show a plurality of embodiments of a digital block.

Independent Claim 37 recites:

A microcontroller circuit, comprising:

a programmable non-volatile memory containing programming code;

a plurality of dynamically programmable analog circuit blocks configured to receive a first subset of said programming data from said programmable memory and wherein said analog circuit blocks are dynamically configurable and programmable to perform a plurality of various analog functions; and

a plurality of dynamically programmable digital circuit blocks configured to receive a second subset of said programming data from said programmable memory, at least a first one of said programmable digital circuit blocks being coupled directly or indirectly to at least a first one of said programmable analog circuit blocks, wherein each dynamically programmable digital circuit block is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation.

Item 10 of Figures 1A and 1B of the instant specification illustrates embodiments of the present invention in accordance with this Claim. Explanation of these items is provided by the instant Specification at least at page 15, line 25, *et seq.*, *inter alia.* In addition, Figure 3 shows the interconnects between analog blocks 20 in an array in accordance with one embodiment of the present invention. Further, Figures 4A, 4B, 5, 6, 7, 8A and 8B, 9A, 9B, 10, 11, 12A, 12B, 13, 14A and 14B show a plurality of

embodiments of an analog block. Still further, Figures 16, 18, 19, 20, 21, 22, 23, and 24 show a plurality of embodiments of a digital block. Figure 16 and the specification at page 46 line 11, *et seq.*, *inter alia*, disclose the claimed embodiment of a "single register write."

Independent Claim 42 recites:

A microcontroller circuit, comprising:

a programmable non-volatile memory containing programming code;

a plurality of dynamically programmable analog circuit blocks configured to receive a first subset of said programming data from said programmable memory and wherein said analog circuit blocks are dynamically configurable and programmable to perform a plurality of various analog functions; and

a plurality of dynamically programmable digital circuit blocks configured to receive a second subset of said programming data from said programmable memory, at least a first one of said programmable digital circuit blocks being coupled directly or indirectly to at least a first one of said programmable analog circuit blocks, wherein each dynamically programmable digital circuit block is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation.

Item 10 of Figures 1A and 1B of the instant specification illustrates embodiments of the present invention in accordance with this Claim. Explanation of these items is provided by the instant Specification at least at

page 15, line 25, *et seq.*, *inter alia.* In addition, Figure 3 shows the interconnects between analog blocks 20 in an array in accordance with one embodiment of the present invention. Further, Figures 4A, 4B, 5, 6, 7, 8A and 8B, 9A, 9B, 10, 11, 12A, 12B, 13, 14A and 14B show a plurality of embodiments of an analog block. Still further, Figures 16, 18, 19, 20, 21, 22, 23, and 24 show a plurality of embodiments of a digital block. Figure 16 and the specification at page 46 line 11, *et seq.*, *inter alia*, disclose the claimed embodiment of a "single register write."

Independent Claim 51 recites:

> A programmable digital circuit in a microcontroller comprising a non-volatile memory and a programmable analog circuit dynamically programmable to perform one or more of a plurality of various analog functions wherein said non-volatile memory stores code for programming said digital and said analog circuit, said programmable digital circuit comprising at least three programmable digital circuit blocks coupled in series and/or in parallel, each programmable digital circuit block being (i) controlled by an n bit register or look up table containing programming information including a cascading bit and (ii) configured to provide at least one of a plurality of digital functions, wherein the cascading bit determines whether a particular programmable digital circuit block is coupled is series with an adjacent programmable digital circuit block, and when programmed, the programmable digital circuit provides at least one digital system

function, wherein each programmable digital circuit block is configurable to perform any one of said digital functions upon being configured with a single register write operation.

Item 10 of Figures 1A and 1B of the instant specification illustrates embodiments of the present invention in accordance with this Claim. Explanation of these items is provided by the instant Specification at least at page 15, line 25, *et seq.*, *inter alia.* In addition, Figure 3 shows the interconnects between analog blocks 20 in an array in accordance with one embodiment of the present invention. Further, Figures 4A, 4B, 5, 6, 7, 8A and 8B, 9A, 9B, 10, 11, 12A, 12B, 13, 14A and 14B show a plurality of embodiments of an analog block. Still further, Figures 16, 18, 19, 20, 21, 22, 23, and 24 show a plurality of embodiments of a digital block. Figure 16 and the specification at page 46 line 11, *et seq.*, *inter alia*, disclose the claimed embodiment of a "single register write."

Independent Claim 52 recites:

A system comprising:

a microcontroller comprising a non-volatile memory;

a subsystem comprising an array of digital components and an array of analog components wherein said analog components are programmable to perform one or more of a plurality of various analog functions and wherein said analog components and said digital

components are programmed with code stored in said non-volatile memory, wherein each digital component is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation; and

a coupling mechanism coupled to said subsystem; wherein selectively, said functionality is configurable to execute a first function according to an input of a first type, said coupling mechanism is configurable to implement a connectability state for said system with which said system is connectable to an external entity according to a user input of a second type.

Item 10 of Figures 1A and 1B of the instant specification illustrates embodiments of the present invention in accordance with this Claim. Explanation of these items is provided by the instant Specification at least at page 15, line 25, *et seq.*, *inter alia.* In addition, Figure 3 shows the interconnects between analog blocks 20 in an array in accordance with one embodiment of the present invention. Further, Figures 4A, 4B, 5, 6, 7, 8A and 8B, 9A, 9B, 10, 11, 12A, 12B, 13, 14A and 14B show a plurality of embodiments of an analog block. Still further, Figures 16, 18, 19, 20, 21, 22, 23, and 24 show a plurality of embodiments of a digital block. Figure 16 and the specification at page 46 line 11, *et seq.*, *inter alia*, disclose the claimed embodiment of a "single register write."

Independent Claim 58 recites:

In a system disposed in an integrated circuit, said system comprising:

a microcontroller comprising a non-volatile program memory;

a subsystem coupled to said non-volatile program memory, comprising a plurality of analog functionalities and of digital functionalities that are both configurable according to a user input wherein said analog functionalities are programmable to perform one or more of a plurality of various analog functions and wherein said analog functionalities and said digital functionalities are programmed with code stored in said non-volatile program memory, wherein each digital functionality is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation;

an interconnecting mechanism configurable for selectively interconnecting said plurality of analog functionalities and said plurality of digital functionalities according to said user input; and

a coupling mechanism coupled to said subsystem that is configurable to implement a connectability state for said system by which said system is connectable to an external entity according to said user input, a method of configuring said system comprising:

a) selecting a function from the list consisting of analog functions, digital functions, and; mixed analog and digital functions

b) selecting an interconnection state to effectuate an interconnection between said analog functionalities and said digital functionalities corresponding to said function;

c) selecting said connectability state to effectuate an connection between said system and an external entity corresponding to said function; and

d) implementing said function, said interconnection state, and said connectability state according to said a), said b) and said c).

Item 10 of Figures 1A and 1B of the instant specification illustrates embodiments of the present invention in accordance with this Claim. Explanation of these items is provided by the instant Specification at least at page 15, line 25, *et seq.*, *inter alia.* In addition, Figure 3 shows the interconnects between analog blocks 20 in an array in accordance with one embodiment of the present invention. Further, Figures 4A, 4B, 5, 6, 7, 8A and 8B, 9A, 9B, 10, 11, 12A, 12B, 13, 14A and 14B show a plurality of embodiments of an analog block. Still further, Figures 16, 18, 19, 20, 21, 22, 23, and 24 show a plurality of embodiments of a digital block. Figure 16 and the specification at page 46 line 11, *et seq.*, *inter alia*, disclose the claimed embodiment of a "single register write."

Grounds of Rejection to be Reviewed on Appeal

Appellants appeal the rejection of Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57-59 under 35 USC § 112, second paragraph.

Appellants appeal the rejection of Claims 1, 37 and 52 under 35 USC § 103(a) over Tzori (US 5,748,875, "Tzori") in view of Insenser Farre et al. (US 5,748,875, "Insenser").

Appellants appeal the rejection of Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57 under 35 USC § 103(a) over Insenser Farre et al., (U.S. Patent No. 6,460,172 "Insenser") in view of Furtek et al., (U.S. Patent No. 5,894,565 "Furtek") and further yet in view of van der Wal et al., (U.S. Patent No. 6,188,381 "van der Wal").

Appellants appeal the rejection of Claims 58-59 under 35 USC § 103(a) over Insenser Farre et al., (U.S. Patent No. 6,460,172 "Insenser") in view of Gamal et al., (U.S. Patent No. 5,754,826 "Gamal") and further in view of van der Wal et al., (U.S. Patent No. 6,188,381 "van der Wal").

Arguments

A. Rejection of Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57-59 under 35 USC § 112, second paragraph.

The rejection states that the "connection between the digital blocks themselves are not being clearly recited," and apparently argues that such lack of a connection amounts to a "gap between the elements." Appellants traverse. For example, Claim 1 recites that a digital functional block is coupled to an interconnect, and that the interconnect is part of a functional unit, and that the functional unit is coupled to a bus.

The Examiner appears to seek connection where none is claimed, e.g., to limit the claimed structure beyond the recited limitations. For example, the rejection asks, "(is there) any direct connection between a first functional unit and (a) second functional unit?" Appellants are unclear as to the meaning of the rejection's term "direct connection," as a "direct connection" between functional units is not defined in the present application, the cited art or the rejection.

Appellants respectfully assert that no such "direct connection" is recited in Claim 1. Thus, embodiments in accordance with the present

claimed invention as recited by Claim 1 may or may not comprise such "direct connections."

Alternatively, Claim 17 recites additional coupling between analog and digital circuit blocks, yet remains rejected under 35 USC § 112, second paragraph.

Appellants respectfully assert that Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57-59 recite that which is novel as well as those necessary structural cooperative relationships of elements necessary to practice the invention, as required by 35 USC § 112. For example, it is well understood to couple a plurality of functional units to a bus, as recited by Claim 1. Further, Claim 1 recites a functional unit coupled to said bus, and the functional unit comprises digital functional blocks. Thus, the coupling of the digital blocks is properly set forth, in contrast to the rejection's allegation.

Appellants respectfully assert that Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57-59 fully comply with 35 USC § 112, and respectfully submit that the rejection is overcome.

B. Rejection of Claims 1, 37 and 52 under 35 USC § 103(a) as being allegedly unpatenable over Tzori (US 5,748,875, "Tzori") in view of Insenser Farre et al. (US 5,748,875, "Insenser")

B1. Improper combination of Tzori in view of Insenser

Appellants respectfully assert that Tzori and Insenser are non-analogous art, and that therefore the proposed combination of Tzori in view of Insenser is improper. Insenser is directed to "a user programmable integrated circuit" (Abstract). In contrast, Tzori is directed to a "digital logic simulation/emulation system." Appellants respectfully assert that one of ordinary skill in the art would not seek to improve Tzori's "digital logic simulation/emulation system" from the field of "user programmable integrated circuits," as taught by Insenser.

As Tzori and Insenser are non-analogous art, Appellants respectfully assert that the proposed combination of Tzori in view of Insenser is improper, and that all rejections dependent upon Tzori in view of Insenser are therefore overcome. For this reason, Appellants respectfully assert that the proposed combination of Tzori in view of Insenser fails to establish *prima facie* obviousness under 35 U.S.C. § 103(a), and respectfully assert that all rejections over Tzori in view of Insenser are overcome.

In addition, Appellants respectfully assert that Tzori is non-analogous art per *In re Clay*, 966 F.2d 656, 659, 23 USPQ2d 1058, 1060-61 (Fed. Cir. 1992). Per *In re Clay*, a reference must "(commend) itself to an inventor's attention in considering his problem." Appellants respectfully assert that Tzori is directed to a "digital logic simulation/emulation system" (Abstract). Appellants do not find the systems of simulation taught by Tzori to commend Tzori to one of ordinary skill in consideration of Appellants' problem. For example, the claims of the present invention are not directed to simulation or emulation of digital logic, as is Tzori.

Appellants respectfully assert that Tzori would not commend itself to one of ordinary skill in the art in consideration of the problems solved by the present invention, due to the myriad well known differences between systems for simulating hardware and actual hardware, as disclosed and claimed in the present application.

Appellants respectfully assert that the citation of Tzori is improper, and that all rejections dependent upon Tzori are therefore overcome. For this reason, Appellants respectfully assert that the basis for rejecting Claims 1, 37 and 52 under 35 U.S.C. § 103(a) is overcome and respectfully assert that these Claims are patentable.

In addition, Appellants respectfully assert that there is no motivation in the cited art to combine Tzori in view of Insenser, as proposed by the rejection. The rejection proposes the modification to "includ(e) the analog blocks as claimed." The language of the rejection indicates that the claims of the present application improperly guided the construction of the rejection. Any such hindsight reasoning is wholly and completely improper.

Moreover, Tzori is directed to a system for simulation/emulation of digital logic (Title, Abstract, *inter alia*, emphasis added). Appellants respectfully assert that one of ordinary skill in the art would not be motivated to improve simulation/emulation of digital logic by the addition of analog function blocks, as proposed by the rejection.

Per *In re Vaeck,* 947 F.2d 488, 493, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991), "[A] proper analysis under § 103 requires, *inter alia*, consideration of... whether the prior art would have suggested to those of ordinary skill in the art that they should make the claimed composition or device, or carry out the claimed process." Regardless of the type of disclosure, the prior art must provide some reason, motivation or suggestion to one of ordinary skill in the art to make the claimed invention in order to support a conclusion of obviousness.

As there is no reason or suggestion in the art to make the proposed modification, Appellants respectfully assert that the rejection implies impermissible hindsight to forge a combination of references guided only by the disclosure and claims of the present application

Further, the proposed addition of analog blocks clearly changes the digital principle of operation of the primary reference. For example, Tzori is directed to a "digital logic simulation/emulation system" (Abstract, emphasis added). Per *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959), "if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious." As the proposed modification changes the principle of operation of the primary reference, the rejection fails to establish *prima facie* obviousness.

For this further reason, Appellants respectfully assert that the proposed combination of Tzori in view of Insenser fails to establish *prima facie* obviousness under 35 U.S.C. § 103(a), and respectfully assert that all rejections over Tzori in view of Insenser are overcome.

Furthermore, the rejection relies upon numerous unjustifiable interpretations of the cited art. For example, the rejection alleges an "IC socket is an integrated circuit." Appellants traverse. As is known to those of ordinary skill in the art, an integrated circuit socket is a mechanical connector that is utilized to accept, remove or replace an integrated circuit. The socket itself has no logic or analog function. Appellants respectfully note that the rejection provides absolutely no documentary or other evidence to support such a baseless allegation.

Moreover, the rejection depends on an allegation that the function of such a socket "can be integrated into microcontroller." Appellants traverse. A microcontroller cannot be used to accept/remove/replace or otherwise connect another integrated circuit device, in the manner of the taught socket. Consequently, the proposed combination must lose at least the function of being able to accept/remove/replace another integrated circuit device. Thus, not only is the rejection's interpretation of the cited art demonstrably incorrect, the proposed modification changes at least the principle of operation of the primary reference of accepting, removing and/or replacing another IC. Per *In re Ratti*, the rejection fails to establish *prima facie* obviousness.

For this additional reason, Appellants respectfully assert that the proposed combination of Tzori in view of Insenser fails to establish *prima facie* obviousness under 35 U.S.C. § 103(a), and respectfully assert that all rejections over Tzori in view of Insenser are overcome.

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B2. Independent Claim 1

With respect to Claim 1, Appellants respectfully assert that the rejection improperly equates Tzori's "Pod 32" with the recited "bus." Importantly, "pod 32" is not described by Tzori as a "bus." As taught by Tzori:

> hardware pod 32... is adapted to receive a digital logic IC by a zero insertion force ("ZIF") IC socket 34. In addition to the IC socket 34, the hardware pod 32 illustrated in FIG. 1 includes two (2) configurable-logic ICs 36a and 36b.
>
> The hardware pod 32 further includes a central processing unit ("CPU") 44 that preferably includes an Integrated Device Technology, Inc., of Santa Clara, Calif. R3081 MIPS R3000 derivative RISC microprocessor together with other ancillary ICs. A microprocessor bus 46 couples the CPU 44 to a read only memory ("ROM") 48, a random access memory ("RAM") 52 and to a communication port 54, which is preferably an Sonic Ethernet IC marketed by National Semiconductor, Inc. of Santa Clara, Calif. The ROM 48, which provides 512K bytes of storage, holds only a minimum computer program required to boot the CPU 44 sufficiently to permit receiving additional computer programs through the communication port 54. (column 8, lines 25-47)

As understood by Appellants, "pod 32" is a printed circuit board comprising, and populated with, at least six integrated circuits and other components, including a socket for accepting another integrated circuit device, as described above and in Figure 1. Appellants respectfully assert that one of ordinary skill in the art would not understand "pod 32" as the recited "bus."

As is known by those of ordinary skill in the art, the recited "bus" does not consist of an "IC socket," "two (2) configurable-logic ICs," "CPU 44," "ROM 48," RAM 52" and "Ethernet IC 54." While Tzori may teach a generic "bus," Tzori teaches that "Pod 32" is not a bus. Consequently, the couplings to the recited "bus," set forth by the limitations of Claim 1, are not and cannot be taught or suggested by "pod 32" as alleged by the rejection.

Appellants respectfully assert that Insenser fails to remedy this deficiency of Tzori, and note that the rejection does not allege such remedy.

For this additional reason, Appellants respectfully assert that the basis for rejecting Claim 1 under 35 U.S.C. § 103(a) is overcome and respectfully assert that this Claim is patentable.

Further with respect to Claim 1, Appellants respectfully assert that Tzori actually teaches away from embodiments of the present claimed

invention, as recited by Claim 1. As understood by Appellants, Tzori uses at least two bus structures to couple the various elements. For example, "microprocessor bus 46 couples the CPU 44 to a read only memory ('ROM') 48, a random access memory ('RAM') 52 and to a communication port 54," while "stimulus/response data-bus 278" couples the CPU 44 to other elements of pod 32. In teaching the use of at least two busses to couple to such varied elements, Tzori actually teaches away from embodiments of the present claimed invention that recite coupling a microprocessor, a memory and a plurality of functional units to a single bus, as recited by Claim 1.

For this further reason, Appellants respectfully assert that the basis for rejecting Claim 1 under 35 U.S.C. § 103(a) is overcome and respectfully assert that this Claim is patentable.

Further still with respect to Claim 1, Appellants respectfully assert that Tzori actually teaches away from embodiments of the present claimed invention, as recited by Claim 1. Claim 1 recites "a microcontroller circuit." As known by those of ordinary skill in the art, a microcontroller is a single integrated circuit device. In contrast, Tzori teaches functions such as a CPU, ROM, RAM, communications and configurable logic in separate integrated circuits.

In teaching the use of multiple integrated circuits, Tzori actually teaches away from embodiments of the present claimed invention that recite a single integrated circuit, as recited by Claim 1. Moreover, Tzori teaches an "IC socket 34" as a part of "pod 32." As is known by those of ordinary skill in the art, such a socket cannot be integrated into the recited "microcontroller." In this additional manner, Tzori again teaches away from embodiments of the present claimed invention that recite a single integrated circuit, as recited by Claim 1.

For these further still reasons, Appellants respectfully assert that the basis for rejecting Claim 1 under 35 U.S.C. § 103(a) is overcome and respectfully assert that this Claim is patentable.

Further yet still with respect to Claim 1, Appellants respectfully assert that Tzori in view of Insenser fails to teach or suggest the claimed limitation "an interconnect wherein said interconnect is dynamically configurable and programmable" as recited by Claim 1. The rejection alleges that Tzori "trace 42" and "data-bus 278" suggest this instant limitation. Appellants respectfully traverse. Appellants find no teaching in Tzori that either "trace 42" or "data-bus 278" is "dynamically configurable and programmable" as recited by Claim 1. Appellants respectfully note that the rejection fails to provide a citation for such alleged teaching. As understood by Appellants,

"trace 42" and "data-bus 278" are merely wiring traces on a printed circuit board. As is well known to those of ordinary skill in the art, printed circuit board traces lack dynamic configuration and programmability.

Appellants respectfully assert that Insenser fails to remedy this deficiency of Tzori, and note that the rejection does not allege such remedy.

For this further yet still reason, Appellants respectfully assert that the basis for rejecting Claim 1 under 35 U.S.C. § 103(a) is overcome and respectfully assert that this Claim is patentable.

Still further with respect to Claim 1, Appellants respectfully assert that Tzori in view of Insenser fails to teach or suggest the claimed limitation "configured with a single register write operation" as recited by Claim 1. While Tzori may teach "load(ing)... configuration data...into the configurable-logic ICs 36a and 36b," Tzori is completely silent as to the number of register write operations required to perform this task. More specifically, Tzori does not teach configuration "with a single register write operation" as recited by Claim 1.

Appellants respectfully assert that Insenser fails to remedy this deficiency of Tzori, and note that the rejection does not allege such remedy.

In fact, with respect to another rejection, in section 18, the rejection concedes, "Insensers [sic] did not specifically showed [sic] single write operation as claimed." Appellants concur with such an acknowledgment.

For this still further reason, Appellants respectfully assert that the basis for rejecting Claim 1 under 35 U.S.C. § 103(a) is overcome and respectfully assert that this Claim is separately patentable for the aforementioned reasons.

B3. Independent Claim 37

Appellants respectfully assert that Claim 37 overcomes the rejections of record for at least the rationale previously presented with respect to Claim 1 in section B2, and respectfully assert that this Claim is patentable.

In addition with respect to Claim 37, Appellants respectfully assert that Tzori in view of Insenser fails to teach or suggest the claimed limitation "a microcontroller circuit... comprising a programmable non-volatile memory," as recited by Claim 37. As previously presented with respect to Claim 1, Tzori does not teach a microcontroller. In contrast, Tzori teaches a system comprising multiple separate integrated circuit devices.

Tzori specifically teaches an external non-volatile program memory, in contrast to the claimed limitation of an internal non-volatile program memory contained within the recited microprocessor: "microprocessor bus 46 couples the CPU 44 to a read only memory ("ROM") 48... and to a communication port 54" (column 8 lines 34-46).

Further, Tzori teaches away from most software being contained within any non-volatile memory: "The ROM 48... holds only a minimum computer program required to boot the CPU 44 sufficiently to permit

receiving additional computer programs through the communication port 54" (column 8 lines 34-46). Thus, in teaching that a non-volatile memory is limited to holding only "boot" code, Tzori teaches away from any non-volatile memory containing "programming data" for the programmable analog or digital circuit blocks, as recited by Claim 37.

As Tzori both leads away and teaches away from these claimed limitations, Appellants respectfully assert that the basis for rejecting Claim 37 under 35 U.S.C. § 103(a) is overcome and respectfully assert that this Claim is separately patentable for the aforementioned reasons.

B4. Independent Claim 52

Appellants respectfully assert that Claim 52 overcomes the rejections of record for at least the rationale previously presented with respect to Claim 1 in section B2, and respectfully assert that this Claim is patentable.

In addition with respect to Claim 52, Appellants respectfully assert that Tzori in view of Insenser fails to teach or suggest the claimed limitation "a microcontroller comprising a non-volatile memory," as recited by Claim 52. As previously presented with respect to Claim 1, Tzori does not teach a microcontroller. In contrast, Tzori teaches a system comprising multiple separate integrated circuit devices.

Tzori specifically teaches an external non-volatile program memory, in contrast to the claimed limitation of an internal non-volatile program memory contained within the recited microprocessor: "microprocessor bus 46 couples the CPU 44 to a read only memory ("ROM") 48... and to a communication port 54" (column 8 lines 34-46).

Further, Tzori leads away from most software being contained within any non-volatile memory: "The ROM 48... holds only a minimum computer program required to boot the CPU 44 sufficiently to permit receiving

additional computer programs through the communication port 54 (column X lines Y-Z). Thus, in teaching that a non-volatile memory is limited to holding only "boot" code, Tzori teaches away the claimed limitation " wherein said analog components and said digital components are programmed with code stored in said non-volatile memory," as recited by Claim 52.

As Tzori teaches away from these claimed limitations, Appellants respectfully assert that the basis for rejecting Claim 52 under 35 U.S.C. § 103(a) is overcome for these additional reasons, and respectfully assert that this Claim is separately patentable for the aforementioned reasons.

C. Rejection of Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57 under 35 USC § 103(a) as being allegedly unpatenable over Insenser Farre et al., (U.S. Patent No. 6,460,172 "Insenser") in view of Furtek et al., (U.S. Patent No. 5,894,565 "Furtek") and further yet in view of van der Wal et al., (U.S. Patent No. 6,188,381 "van der Wal")

C1. Improper combination in view of van der Wal

Appellants respectfully assert that van der Wal is non-analogous art per *In re Clay*, 966 F.2d 656, 659, 23 USPQ2d 1058, 1060-61 (Fed. Cir. 1992). Per *In re Clay*, a reference must "(commend) itself to an inventor's attention in considering his problem." Appellants respectfully assert that van der Wal is directed to a "real time modular video processing system" (Abstract). Appellants do not find the video processing systems taught by van der Wal to commend van der Wal to one of ordinary skill in the art in consideration of Appellants' problem. For example, the claims of the present invention are not directed to video processing.

Appellants respectfully assert that van der Wal would not commend itself to one of ordinary skill in the art in consideration of the problems solved by the present invention, due to the myriad well known differences between

video processing systems and configurable microcontrollers, as disclosed and claimed in the present application.

Appellants respectfully assert that the citation of van der Wal is improper. For this reason, Appellants respectfully assert that the proposed combination of Insenser in view of Furtek and further yet in view of van der Wal fails to establish *prima facie* obviousness under 35 U.S.C. § 103(a), and respectfully assert that all rejections over Insenser in view of Furtek and further yet in view of van der Wal are overcome.

C2. Independent Claim 1

With respect to Claim 1, Appellants respectfully assert that Insenser in view of Furtek and further yet in view of van der Wal fails to teach or suggest the claimed limitation of a bus coupling a non-volatile memory and a plurality of functional units (further limited), as recited by Claim 1. The rejection alleges that Insenser's "optimized interface 9" is such a bus. Appellants respectfully traverse.

Insenser teaches, "optimized interface 9 (connects) the microprocessor core to the programmable cells and other on-chip peripherals 10" (column 2 lines 14-25). Importantly, "optimized interface 9" is not taught to couple the memory. Consequently, in consideration of all the limitations of bus coupling recited in Claim 1, "optimized interface 9" does not suggest the recited "bus." Moreover, no teaching of Insenser meets the claimed limitations of a "bus" as recited by Claim 1.

Appellants respectfully assert that neither Furtek nor van der Wal remedies this deficiency of Insenser, and note that the rejection does not allege such remedy.

For this reason, Appellants respectfully assert that the basis for rejecting Claim 1 under 35 U.S.C. § 103(a) is overcome, and respectfully assert that this Claim is patentable.

Further with respect to Claim 1, Appellants respectfully assert that Insenser in view of Furtek and further still in view of van der Wal fails to teach or suggest the claimed limitation of a non-volatile memory coupled to a bus, as recited by Claim 1. The rejection concedes that Insenser "did not specifically showed [sic] the non-volatile memory as claimed." Appellants concur with such an acknowledgment.

To correct this deficiency of Insenser, the rejection proposes to use the non-volatile memory 83 of Furtek. However, "dedicated function element 83" is placed "at the corners of each block 15 of logic cells 11 in the space provided at the intersections of rows and columns of repeaters 27 bounding the blocks 15" (column 11, lines 57-67). Appellants respectfully assert that the non-volatile memory taught by Furtek is ill-suited in both construction and logical placement for the function required by Insenser. Further, the bus (95, 86) taught by Furtek in relation to function element 83, is not taught to be coupled to elements external to the FPGA circuit. Thus, Furtek fails to teach or suggest a non-volatile memory coupled as recited to the remaining claimed elements recited by Claim 1.

In addition, Insenser requires data and programs stored in changeable memory, e.g., RAM: "RAM memory 1 for data and programs" (column 3 line 15). Consequently, the proposed replacement would render the primary reference incapable of performing its intended function. For example, data stored in a non-volatile ROM of Furtek cannot be accessed or changed, as required by Insenser.

Per *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959), "if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious."

As the proposed modification of Insenser in view of Furtek fails to establish *prima facie* obviousness, Appellants respectfully assert that all rejections dependent upon van Insenser in view of Furtek are therefore overcome. For this reason, Appellants respectfully assert that Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57 overcome the rejections of record, and respectfully solicit allowance of these Claims.

Still further with respect to Claim 1, Appellants respectfully assert that Insenser in view of Furtek and further yet in view of van der Wal fails to teach or suggest the claimed limitation of a "a dynamically configurable and programmable digital functional block coupled to said interconnect, wherein said dynamically configurable and programmable digital functional block is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation," as recited by Claim 1. The rejection concedes that "Insensers [sic] did not specifically showed [sic] single write operation as claimed." Appellants concur with such an acknowledgment.

To correct this deficiency of Insenser, the rejection proposes to use a write operation taught by van der Wal.

The cited passage (Col. 10, lines 30-38) of van der Wal recites:

> These 10 bits represent the 8 bits of data and 2 bits of HA and VA timing in the format described above. In a preferred embodiment, the crosspoint switch 202 is implemented using 10 I-CUBE IQ96 crosspoint switch devices. Each of these devices provides a reconfigurable crosspoint switch for a single bit of the 10 bits of video data. These devices are configured so one control register write is capable of switching all 10 bits of data in all 10 IQ96 devices simultaneously. (emphasis added)

Appellants respectfully assert that the rejection misinterprets this disclosure as teaching the configuration or reconfiguration of a device with a single register write, as in Independent Claim 1. In contrast, Appellants assert that this cited passage is directed to one control register write that is capable of switching all bits of video data in all devices simultaneously.

Importantly, the cited passage assumes that the devices are already configured, without addressing a method of configuration. Thus, the cited passage teaches functionality of a configured device, but does not teach configuration.

According to the passage, 10 (ten) I-CUBE IQ96 crosspoint switch devices implement the crosspoint switch 202. Moreover, each I-CUBE IQ96 crosspoint switch device provides a reconfigurable crosspoint switch for a single bit of the 10 bits of video data. Further, the 10 (ten) I-CUBE IQ96 crosspoint switch devices are configured as a whole in a manner described by the phrase which begins after the word "so" in the last sentence of the passage. That is, the phrase, "one control register write is capable of switching all 10 bits of [video] data in all 10 IQ96 devices simultaneously" (emphasis added), refers to the operation of the 10 (ten) I-CUBE IQ96 crosspoint switch devices as a whole.

Thus, there is no support for the rejection's assertion that the passage teaches, "single control register write for reconfiguring all functional blocks or devices." The one control register write in the passage is described as being capable of switching all 10 bits of video data in all 10 IQ96 devices simultaneously instead of reconfiguring functional blocks or devices. While the passage notes that bits of video data are switched simultaneously with the one control register write, the passage fails to describe any relationship between the one control register write and configuration (or reconfiguration) of the individual I-CUBE IQ96 crosspoint switch device. Use of the term "switching" corresponds to each I-CUBE IQ96 crosspoint switch device having an "on state" and an "off state."

Therefore, each I-CUBE IQ96 crosspoint switch device must be configured/reconfigured with respect to its input and output ports via its corresponding control register in some manner that is neither described nor expressly/implicitly suggested as being a single control register write. Thus, van der Wal does not teach or suggest that a digital functional block is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation, as in the claimed embodiment of Independent Claim 1.

For this still further reason, Appellants respectfully assert that the basis for rejecting Claim 1 under 35 U.S.C. § 103(a) is overcome, and respectfully assert that this Claim is patentable.

C3. Claims depending from Claim 1

Appellants respectfully assert that Claims 2 – 10 overcome the rejections of record by virtue of their dependency, and respectfully submit that these Claims are patentable.

In addition with respect to Claims 4 and 7, Appellants respectfully assert that Insenser in view of Furtek and further yet in view of van der Wal fails to teach or suggest the claimed limitation of "user input" as recited by Claims 4 and 7. The cited references are silent as to user interaction.

For this additional reason, Appellants respectfully assert that Claims 4 and 7 overcome the rejections of record, and respectfully submit that these Claims are separately patentable.

In addition with respect to Claim 9, Appellants respectfully assert that Insenser in view of Furtek and further yet in view of van der Wal fails to teach or suggest the claimed limitation of "wherein said (non-volatile) memory further comprises a random access memory" as recited by Claim 9. As is known to those of ordinary skill in the art, a random access memory, or RAM, generally may be written to without a separate erase operation. For example, read only memories (ROM) are not generally considered to be RAM.

In addition, any element, e.g., a word, of a random access memory may generally be read or written, without having to read or write a larger partition, e.g., a segment or block.

Any RAM memories taught by the cited references are not taught to be non-volatile. Any ROM memories taught by the cited references are not taught to be random access, as ROMs may not be written. Thus, none of the memories that may be taught by the cited references, alone or in combination, are taught or suggested to be non-volatile random access memories. Further, Insenser in view of Furtek and further yet in view of van der Wal fails to teach or suggest all of the remaining claimed limitations related to the claimed non-volatile random access memory.

For this additional reason, Appellants respectfully assert that Claim 9 overcomes the rejections of record, and respectfully submit that this Claim is separately patentable.

C4. Independent Claims 11, 17, 35, 37, 42, 51, and 52

Appellants respectfully assert that Independent Claims 11, 17, 35, 37, 42, 51, and 52 overcome the rejections of record for at least the rationales previously presented with respect to Claim 1 in section C2. More particularly, Independent Claims 11, 17, 35, 37, 42, 51, and 52, are directed to digital logic whose digital function is "configured with a single register write operation." Appellants respectfully assert that Insenser in view of Furtek and further yet in view of van der Wal fails to teach or suggest this instant limitation, as previously presented with respect to Claim 1 in section C2.

For this reason, Appellants respectfully assert that Claims 11, 17, 35, 37, 42, 51, and 52 overcome the rejections of record, and respectfully submit that these Claims are patentable.

C5. Claims depending from Claims 11, 17, 35, 37, 42, 51, and 52

Appellants respectfully assert that Claims 13-16, 18, 20-21, 23-34, 36, 38-41, 43-49, and 57 overcome the rejections of record by virtue of their dependency, and respectfully submit that these Claims are patentable.

In addition with respect to Claims 13-16, Appellants respectfully assert that Insenser in view of Furtek and further yet in view of van der Wal fails to teach or suggest the claimed limitation of "user input" as recited by Claims 13-16. The cited references are silent as to user interaction.

For this additional reason, Appellants respectfully assert that Claims 13-16 overcome the rejections of record, and respectfully submit that these Claims are separately patentable.

In addition with respect to Claims 20 and 36, the rejection improperly equates "probing" as taught by Insenser with the recited coupling of programmable digital circuit blocks and programmable analog circuit blocks. In fact, the rejection incorrectly characterizes Insenser's teaching. The rejection alleges Insenser to teach, "digital circuit blocks could (be) probed with the analog circuit." Appellants do not find such teaching in Insenser,

and fail to understand how an analog circuit could probe a digital circuit, as alleged.

In contrast, Insenser actually teaches, "[a]ny point inside the digital blocks or the analog subsystems can be probed (by the microprocessor)." (column 3 lines 41-44). Appellants respectfully assert that "probing" by a microprocessor does not teach or suggest coupling programmable digital circuit blocks to programmable analog circuit blocks, as recited by 20 and 36. For example, a teaching of probing either digital or analog blocks fails to suggest coupling the digital blocks to the analog blocks.

For this additional reason, Appellants respectfully assert that Claims 20 and 36 overcome the rejections of record, and respectfully submit that these Claims are separately patentable.

D. Rejection of Claims 58-59 under 35 U.S.C. 103(a) as being unpatentable over Insenser Farre et al., (U.S. Patent No. 6,460,172 "Insenser") in view of Gamal et al., (U.S. Patent No. 5,754,826 "Gamal") and further in view of van der Wal et al., (U.S. Patent No. 6,188,381 "van der Wal").

D1. Improper combination in view of van der Wal

Appellants respectfully reiterate the arguments against modification in view of van der Wal, as previously presented in section C1.

For this reason, Appellants respectfully assert that the proposed combination of Insenser in view of Gamal and further yet in view of van der Wal fails to establish *prima facie* obviousness under 35 U.S.C. § 103(a), and respectfully assert that all rejections over Insenser in view of Gamal and further yet in view of van der Wal are overcome.

D2. Independent Claim 58

With respect to Claim 58, Appellants respectfully assert that Insenser in view of Gamal and further in view of van der Wal fails to teach or suggest the claimed limitation of "a dynamically configurable and programmable digital functional block coupled to said interconnect, wherein said dynamically configurable and programmable digital functional block is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation," as recited by Claim 1. The rejection concedes that "neither Insensers [sic] nor Gammal [sic] showed single write operation as claimed." Appellants concur with such an acknowledgment.

To correct this deficiency of Insenser and Gamal, the rejection proposes to use a write operation taught by van der Wal.

The cited passage (Col. 10, lines 30-38) of van der Wal recites:

> These 10 bits represent the 8 bits of data and 2 bits of HA and VA timing in the format described above. In a preferred embodiment, the crosspoint switch 202 is implemented using 10 I-CUBE IQ96 crosspoint switch devices. Each of these devices provides a reconfigurable crosspoint switch for a single bit of the 10 bits of video

data. These devices are configured so one control register write is capable of switching all 10 bits of data in all 10 IQ96 devices simultaneously. (emphasis added)

Appellants respectfully assert that the rejection misinterprets this disclosure as teaching the configuration or reconfiguration of a device with a single register write, as recited in Independent Claim 58. In contrast, as understood by Appellants, this cited passage is directed to one control register write that is capable of switching all bits of video data in all devices simultaneously.

Importantly, the cited passage assumes that the devices are already configured, without addressing a method of configuration. Thus, the cited passage teaches functionality of a configured device, but does not teach configuration.

According to the passage, 10 (ten) I-CUBE IQ96 crosspoint switch devices implement the crosspoint switch 202. Moreover, each I-CUBE IQ96 crosspoint switch device provides a reconfigurable crosspoint switch for a single bit of the 10 bits of video data. Further, the 10 (ten) I-CUBE IQ96 crosspoint switch devices are configured as a whole in a manner described by the phrase which begins after the word "so" in the last sentence of the passage. That is, the phrase, "one control register write is capable of

switching all 10 bits of [video] data in all 10 IQ96 devices simultaneously" (emphasis added), refers to the operation of the 10 (ten) I-CUBE IQ96 crosspoint switch devices as a whole.

Thus, there is no support for the rejection's assertion that the passage teaches, "single control register write for reconfiguring all functional blocks or devices." The one control register write in the passage is described as being capable of switching all 10 bits of video data in all 10 IQ96 devices simultaneously instead of reconfiguring functional blocks or devices. While the passage notes that bits of video data are switched simultaneously with the one control register write, the passage fails to describe any relationship between the one control register write and configuration (or reconfiguration) of the individual I-CUBE IQ96 crosspoint switch device. Use of the term "switching" corresponds to each I-CUBE IQ96 crosspoint switch device having an "on state" and an "off state."

Therefore, each I-CUBE IQ96 crosspoint switch device must be configured/reconfigured with respect to its input and output ports via its corresponding control register in some manner that is neither described nor expressly/implicitly suggested as being a single control register write. Thus, van der Wal does not teach or suggest that a digital functional block is configurable to perform any one of a plurality of predetermined digital

functions upon being configured with a single register write operation, as in the embodiment of Independent Claim 58.

For this additional reason, Appellants respectfully assert that Claim 58 overcomes the rejections of record, and respectfully submit that this Claim is separately patentable.

D3. Dependent Claim 59

Appellants respectfully assert that Claim 59 overcome the rejections of record by virtue of their dependency, and respectfully solicit allowance of these Claims.

In addition with respect to Claim 59, Appellants respectfully assert that the combination of references fails to teach or suggest the claimed limitation of a "time base" as recited by Claim 59. The rejection improperly equates "operating frequency of filters" as taught by Insenser with the recited "time base."

Appellants respectfully assert that the taught "operating frequency of filters" is unrelated to the recited "time base," as understood by those of ordinary skill in the art, and thus fails to teach or suggest the claimed limitation of a "time base," as recited by Claim 59. For this additional reason, Appellants respectfully assert that Claim 59 overcomes the rejections of record, and respectfully submit that this Claim is separately patentable.

Conclusions

Appellants believe that pending Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57-59 are patentable over the cited art. Appellants respectfully request that the rejection of these claims be reversed.

Respectfully submitted,

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I hereby certify that this correspondence is being electronically transmitted to the USPTO via EFS on the date shown below:
January 22, 2008

Donna Petford

Claims Appendix

1. (previously presented) A microcontroller circuit comprising:

a bus;

a microprocessor coupled to said bus;

a memory coupled to said bus, wherein said memory comprises a non-volatile memory; and

a plurality of functional units coupled to said bus, wherein said non-volatile memory functions to program said functional units and wherein said plurality of functional units comprise:

an interconnect wherein said interconnect is dynamically configurable and programmable;

an analog functional block coupled to said interconnect wherein said analog function block is dynamically configurable and programmable to perform one or more of a plurality of various analog functions; and

a dynamically configurable and programmable digital functional block coupled to said interconnect, wherein said dynamically configurable and programmable digital functional block is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation.

2. (Previously Presented) The microcontroller circuit as recited in Claim 1, wherein said memory comprises an erasable memory.

3. (previously presented) The microcontroller circuit as recited in Claim 1, wherein said functional units further comprise a programmable input/output coupling.

4. (previously presented) The microcontroller circuit as recited in Claim 1, wherein a component of said circuit is dynamically programmable according to an user input.

5. (Previously Presented) The microcontroller circuit as recited in Claim 4, wherein said component is selected from the list consisting of said interconnect, said analog functional block, and said digital functional block.

6. (Previously Presented) The microcontroller circuit as recited in Claim 5, wherein a function of said circuit is programmable.

7. (Previously Presented) The microcontroller circuit as recited in Claim 6, wherein said function corresponds to a configuration state.

8. (Previously Presented) The microcontroller circuit as recited in Claim 7, wherein said configuration state is configured according to said user input.

9. (Previously Presented) The microcontroller circuit as recited in Claim 1, wherein said memory further comprises a random access memory.

10. (Previously Presented) The microcontroller circuit as recited in Claim 1, wherein said non-volatile memory comprises a programmable memory.

11. (previously presented)An integrated circuit comprising:

a bus;

a microprocessor coupled to said bus;

a memory coupled to said bus, wherein said memory comprises a non-volatile memory;

a plurality of functional units coupled to said bus, wherein said non-volatile memory stores code for programming said functional units and wherein said plurality of functional units comprise:

an interconnect wherein said interconnect is dynamically configurable and programmable;

an analog functional block coupled to said interconnect wherein said analog function block is dynamically configurable and programmable to perform one or more of a plurality of various analog functions; and

a dynamically configurable and programmable digital functional block coupled to said interconnect, wherein said dynamically configurable and programmable digital functional block is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation; and

an input/output coupling, wherein said integrated circuit comprises a microcontroller.

12. (Canceled)

13. (Original) The circuit as recited in Claim 11, wherein said programmable component is programmable according to a user input.

14. (Original) The circuit as recited in Claim 13, wherein a function of said circuit is programmable.

15. (Original) The circuit as recited in Claim 14, wherein said function corresponds to a configuration state.

16. (Original) The circuit as recited in Claim 15, wherein said configuration state is configured according to said user input.

17. (Previously Presented) A microcontroller circuit, comprising:

a microprocessor;

a plurality of analog circuit blocks wherein said analog function block is dynamically configurable and programmable to perform one or more of a plurality of various analog functions;

a plurality of dynamically programmable digital circuit blocks wherein at least one of said dynamically programmable digital circuit blocks is coupled directly or indirectly to at least one of said dynamically programmable analog circuit blocks wherein at least a first one of said dynamically programmable digital circuit blocks is coupled directly or indirectly to at least a first one of said dynamically programmable analog circuit blocks, and at least a second one of said dynamically programmable digital circuit blocks and said dynamically programmable analog circuit blocks is coupled directly or indirectly to said microprocessor and wherein said coupling is achieved with an interconnect, wherein said interconnect is dynamically programmable and configurable, wherein each dynamically programmable digital circuit block is configurable to perform any one of a plurality of digital functions upon being configured with a single register write operation; and

a programmable non-volatile memory coupled directly or indirectly to said plurality of dynamically programmable digital circuit blocks and said plurality of dynamically programmable analog circuit blocks, said

programmable non-volatile memory storing code for programming at least one of said programmable digital circuit blocks and at least one of said plurality of programmable analog circuit blocks.

18. (Previously Presented) The microcontroller circuit as recited in Claim 17, wherein each of said plurality of dynamically programmable digital circuit blocks is dynamically configured to provide at least one of said digital functions.

19. (Canceled)

20. (Previously Presented) The microcontroller circuit as recited in Claim 17, wherein at least a third one of said programmable digital circuit blocks is coupled to a fourth one of said programmable digital circuit blocks, and at least a third one of said programmable analog circuit blocks is coupled to a fourth one of said programmable analog circuit blocks.

21. (Previously Presented) The microcontroller circuit as recited in Claim 20, wherein a programmed combination of said plurality of programmable digital circuit blocks and said programmable analog circuit blocks is configured to provide at least one digital and/or analog system function.

22. (Canceled)

23. (Previously Presented) The microcontroller circuit as recited in Claim 17, wherein said programmable memory comprises an erasable and programmable memory.

24. (Previously Presented) The microcontroller circuit as recited in Claim 23, wherein said programmable memory comprises an electrically erasable and programmable memory.

25. (Previously Presented) The microcontroller circuit as recited in Claim 17, further comprising a plurality of dynamically programmable and configurable input and/or output blocks, coupled directly or indirectly to at least one of said programmable memory, said programmable digital circuit blocks, said plurality of programmable analog circuit blocks, and said microprocessor.

26. (Previously Presented) The microcontroller circuit as recited in Claim 25, wherein at least a first one of said plurality of dynamically programmable and configurable input and/or output blocks couples one or more external signals to said microprocessor.

27. (Previously Presented) The microcontroller circuit as recited in Claim 26, wherein at least a second one of said plurality of dynamically programmable and configurable input and/or output blocks couples one or more external signals to at least one of said programmable digital circuit blocks and said plurality of programmable analog circuit blocks.

28. (Previously Presented) The microcontroller circuit as recited in Claim 27, wherein at least said second one of said plurality of dynamically programmable and configurable input and/or output blocks couples one or more external signals to at least one of said plurality of programmable analog circuit blocks.

29. (Previously Presented) The microcontroller circuit as recited in Claim 28, wherein said at least one of said plurality of programmable analog circuit blocks send signals to at least one of said programmable digital circuit blocks.

30. (Previously Presented) The microcontroller circuit as recited in Claim 27, wherein at least a third one of said plurality of input and/or output blocks sends data to said programmable memory.

31. (Previously Presented) The microcontroller circuit as recited in Claim 27, further comprising a plurality of registers configured to store programming data for said plurality of programmable digital circuit blocks.

32. (Previously Presented) The microcontroller circuit as recited in Claim 27, further comprising a plurality of latches configured to store programming data for said plurality of programmable analog circuit blocks.

33. (Previously Presented) The microcontroller circuit as recited in Claim 27, further comprising a global routing matrix configured to couple said plurality of input and/or output blocks to said plurality of programmable digital circuit blocks and said plurality of programmable analog circuit blocks.

34. (Previously Presented) The microcontroller circuit as recited in Claim 27, further comprising a system macro routing matrix configured to couple a subset of said plurality of programmable digital circuit blocks to a subset of said plurality of programmable analog circuit blocks.

35. (Previously Presented) A microcontroller circuit, comprising:

a plurality of input and/or output blocks;

a plurality of programmable analog circuit blocks, wherein said analog circuit blocks are dynamically configurable and programmable to perform one or more of a plurality of various analog functions; and

a plurality of dynamically programmable digital circuit blocks, at least one of said programmable digital circuit blocks being coupled directly or indirectly to at least one of said programmable analog circuit blocks wherein at least one of said programmable digital circuit blocks and said programmable analog circuit blocks is coupled directly or indirectly to at least one of said input and/or output blocks, wherein each dynamically programmable digital circuit block is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation; and

a programmable non-volatile memory coupled to said plurality of programmable digital circuit blocks and said plurality of programmable analog circuit blocks, said programmable memory comprising data for programming at least one of said programmable digital circuit blocks and at least one of said plurality of programmable analog circuit blocks.

36. (Previously Presented) The circuit as recited in Claim 35, wherein at least a first one of said plurality of input and/or output blocks sends signals to at least a first one of said plurality of programmable analog circuit blocks, said first programmable analog circuit block sends signals to at

least a first one of said plurality of programmable digital circuit blocks, and said first programmable digital circuit block sends signals to a same or different one of said plurality of input and/or output blocks.

37. (Previously Presented) A microcontroller circuit, comprising:

a programmable non-volatile memory containing programming code;

a plurality of dynamically programmable analog circuit blocks configured to receive a first subset of said programming data from said programmable memory and wherein said analog circuit blocks are dynamically configurable and programmable to perform a plurality of various analog functions; and

a plurality of dynamically programmable digital circuit blocks configured to receive a second subset of said programming data from said programmable memory, at least a first one of said programmable digital circuit blocks being coupled directly or indirectly to at least a first one of said programmable analog circuit blocks, wherein each dynamically programmable digital circuit block is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation.

38. (Previously Presented) The circuit as recited in Claim 37, wherein a second one of said plurality of programmable analog circuit blocks

is coupled to at least one of said first programmable analog circuit block and a second one of said plurality of programmable digital circuit blocks.

39. (Previously Presented) The circuit as recited in Claim 37, wherein a second one of said plurality of programmable digital circuit blocks is coupled to at least one of said first programmable digital circuit block and a second one of said plurality of programmable analog circuit blocks.

40. (Previously Presented) The circuit as recited in Claim 38, wherein said second programmable analog circuit block is coupled to said first programmable analog circuit block and second one of said plurality of programmable digital circuit blocks is coupled to said first programmable digital circuit block.

41. (Previously Presented) The circuit as recited in Claim 38, wherein said second programmable analog circuit block is coupled to said second programmable digital circuit block.

42. (Previously Presented) A microcontroller circuit, comprising:

a plurality of analog circuit blocks wherein said analog circuit blocks are dynamically programmable and configurable to perform one or more of a plurality of various analog functions;

a plurality of programmable digital circuit blocks configured to provide at least one of a plurality of digital functions, wherein each programmable digital circuit block is configurable to perform any one of said digital functions upon being configured with a single register write operation;

a routing matrix configured to couple a subset of said plurality of programmable analog circuit blocks to a first subset of said plurality of programmable digital circuit blocks, at least a first one of said programmable analog circuit blocks being coupled to at least a first one of said programmable digital circuit blocks; and

a programmable non-volatile memory coupled directly or indirectly to said plurality of programmable digital circuit blocks and said plurality of programmable analog circuit blocks, said programmable memory comprising data for programming at least one of said programmable digital circuit blocks and at least one of said plurality of programmable analog circuit blocks.

43. (Previously Presented) The circuit as recited in Claim 42, wherein when programmed, each of said plurality of programmable analog circuit blocks provides at least one of said plurality of analog functions.

44. (Previously Presented) The circuit as recited in Claim 42, wherein when programmed, each programmable digital circuit blocks provides at least one of said digital functions.

45. (Previously Presented) The circuit as recited in Claim 43, wherein when programmed, said plurality of programmable analog circuit blocks and said plurality of programmable digital circuit blocks provides at least one digital and/or analog function.

46. (Previously Presented) The circuit as recited in Claim 42, wherein when programmed, said routing matrix couples a second one of said subset of said plurality of programmable analog circuit blocks to a second one of said subset of said plurality of programmable digital circuit blocks.

47. (Previously Presented) The circuit as recited in Claim 42, wherein said plurality of programmable analog circuit blocks comprises a matrix of n by m analog configurable system macros, n and m independently being an integer of at least two.

48. (Previously Presented) The circuit as recited in Claim 47, wherein each of said analog configurable system macros is configured to provide one or more analog functions selected from the group consisting of a gain function, a comparator function, a switched capacitor function, a filter function, an analog to digital conversion function, a digital to analog conversion function, and an amplifier function.

49. (Previously Presented) The circuit as recited in Claim 42, wherein at least two of said plurality of programmable digital circuit blocks are coupled in series to provide a digital system function.

50. (Canceled)

51. (Previously Presented) A programmable digital circuit in a microcontroller comprising a non-volatile memory and a programmable analog circuit dynamically programmable to perform one or more of a plurality of various analog functions wherein said non-volatile memory stores code for programming said digital and said analog circuit, said programmable digital circuit comprising at least three programmable digital circuit blocks coupled in series and/or in parallel, each programmable digital circuit block being (i) controlled by an n bit register or look up table containing programming information including a cascading bit and (ii) configured to provide at least one of a plurality of digital functions, wherein the cascading bit determines whether a particular programmable digital circuit block is coupled is series with an adjacent programmable digital circuit block, and when programmed, the programmable digital circuit provides at least one digital system function, wherein each programmable digital circuit block is

configurable to perform any one of said digital functions upon being configured with a single register write operation.

52. (Previously Presented) A system comprising:

a microcontroller comprising a non-volatile memory;

a subsystem comprising an array of digital components and an array of analog components wherein said analog components are programmable to perform one or more of a plurality of various analog functions and wherein said analog components and said digital components are programmed with code stored in said non-volatile memory, wherein each digital component is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation; and

a coupling mechanism coupled to said subsystem; wherein selectively, said functionality is configurable to execute a first function according to an input of a first type, said coupling mechanism is configurable to implement a connectability state for said system with which said system is connectable to an external entity according to a user input of a second type.

53-56. (Canceled)

57. (Previously Presented) The system as recited in Claim 52, further comprising a timing functionality, which is configurable to generate a plurality of time bases according to a user input of a third type.

58. (Previously Presented) In a system disposed in an integrated circuit, said system comprising:

a microcontroller comprising a non-volatile program memory;

a subsystem coupled to said non-volatile program memory, comprising a plurality of analog functionalities and of digital functionalities that are both configurable according to a user input wherein said analog functionalities are programmable to perform one or more of a plurality of various analog functions and wherein said analog functionalities and said digital functionalities are programmed with code stored in said non-volatile program memory, wherein each digital functionality is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation;

an interconnecting mechanism configurable for selectively interconnecting said plurality of analog functionalities and said plurality of digital functionalities according to said user input; and

a coupling mechanism coupled to said subsystem that is configurable to implement a connectability state for said system by which said system is

connectable to an external entity according to said user input, a method of configuring said system comprising:

a) selecting a function from the list consisting of analog functions, digital functions, and; mixed analog and digital functions

b) selecting an interconnection state to effectuate an interconnection between said analog functionalities and said digital functionalities corresponding to said function;

c) selecting said connectability state to effectuate an connection between said system and an external entity corresponding to said function; and

d) implementing said function, said interconnection state, and said connectability state according to said a), said b) and said c).

59. (Original) The method as recited in Claim 58, wherein said system further comprises a timing functionality configurable to generate a plurality of time bases, said method further comprising:

selecting a timing base from said plurality of timing bases; and implementing said timing base accordingly.

Evidence Appendix

None.

Related Proceedings Appendix

None.